

The diagram illustrates a fully differential current-mode class-AB output stage. The circuit is powered by a VCC supply and a GND reference. A feedback loop is formed by an error amplifier (labeled 'ERROR AMP') with non-inverting input (+) connected to the output node (VOUT) through resistor R3, and inverting input (-) connected to a reference voltage (VREF) through resistor R4. The error amplifier's output drives a differential pair of PMOS transistors (P0 and P1) and a differential pair of NMOS transistors (N1 and N2). The PMOS transistors (P0, P1) have their sources connected to GND through a switch SW1. The NMOS transistors (N1, N2) have their sources connected to GND through resistors R1 and R2. The gates of P0 and P1 are connected to a common-mode feedback network consisting of a PMOS transistor (P2) and a resistor (R6) in parallel, which is then connected to a resistor (R7) leading to VCC. The gates of N1 and N2 are connected to a common-mode feedback network consisting of an NMOS transistor (N2) and a resistor (R2) in parallel, which is then connected to a resistor (R7) leading to VCC. The output node (VOUT) is connected to the load (LOAD) through a switch SW2. The load is represented by a parallel combination of a resistor (R5) and a capacitor (C0). The output current (IOUT) is shown flowing out of the output node. The circuit also includes a current source (P6) connected to VCC and a current source (N6) connected to GND, both controlled by a common-mode feedback signal (VSC). The current source (P6) is connected to the gates of P0 and P1, and the current source (N6) is connected to the gates of N1 and N2. The current source (P6) is also connected to a reference current (IREF1) and the current source (N6) is connected to a reference current (IREF2).

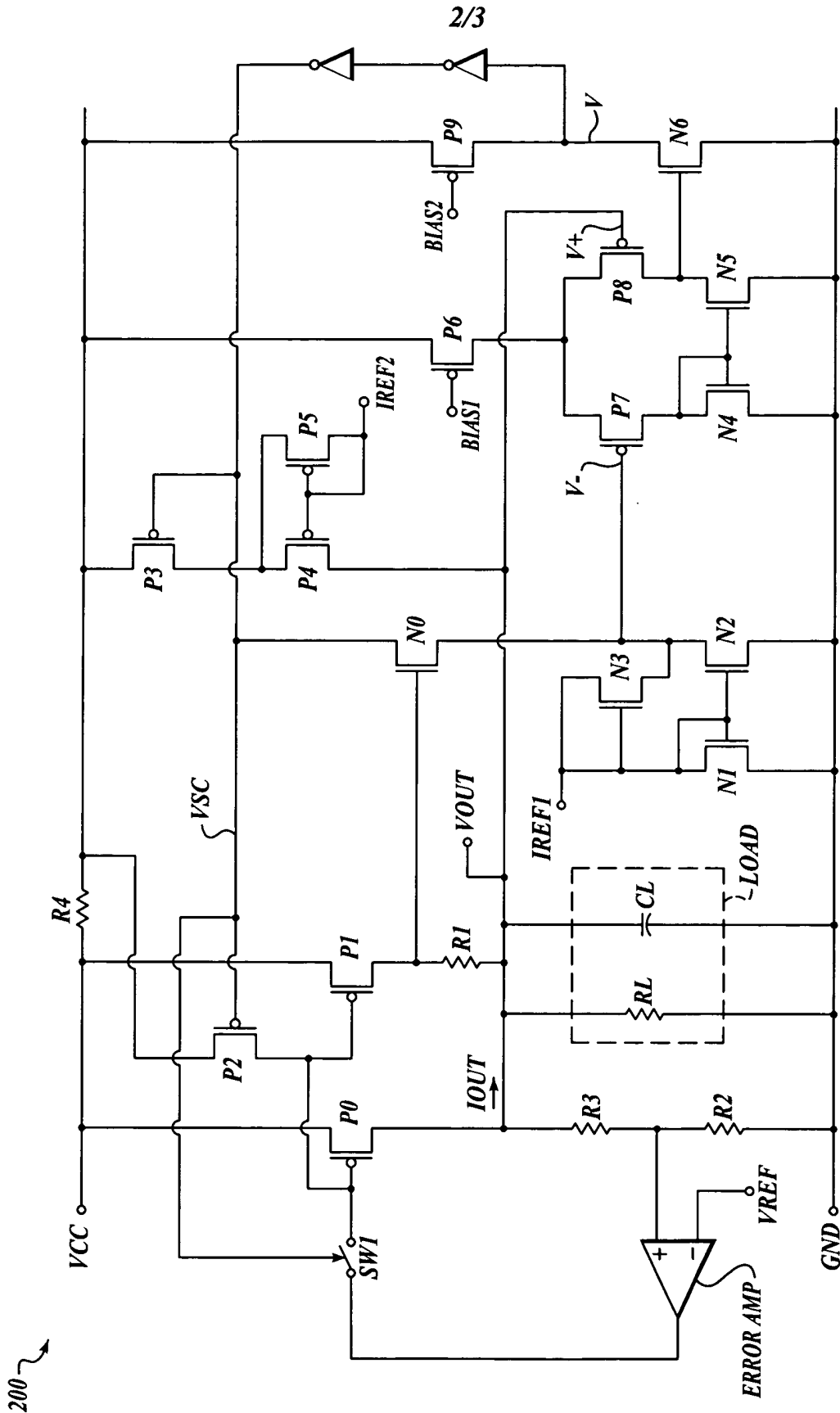


FIGURE 2



Title: OVER-CURRENT PROTECTION CIRCUIT

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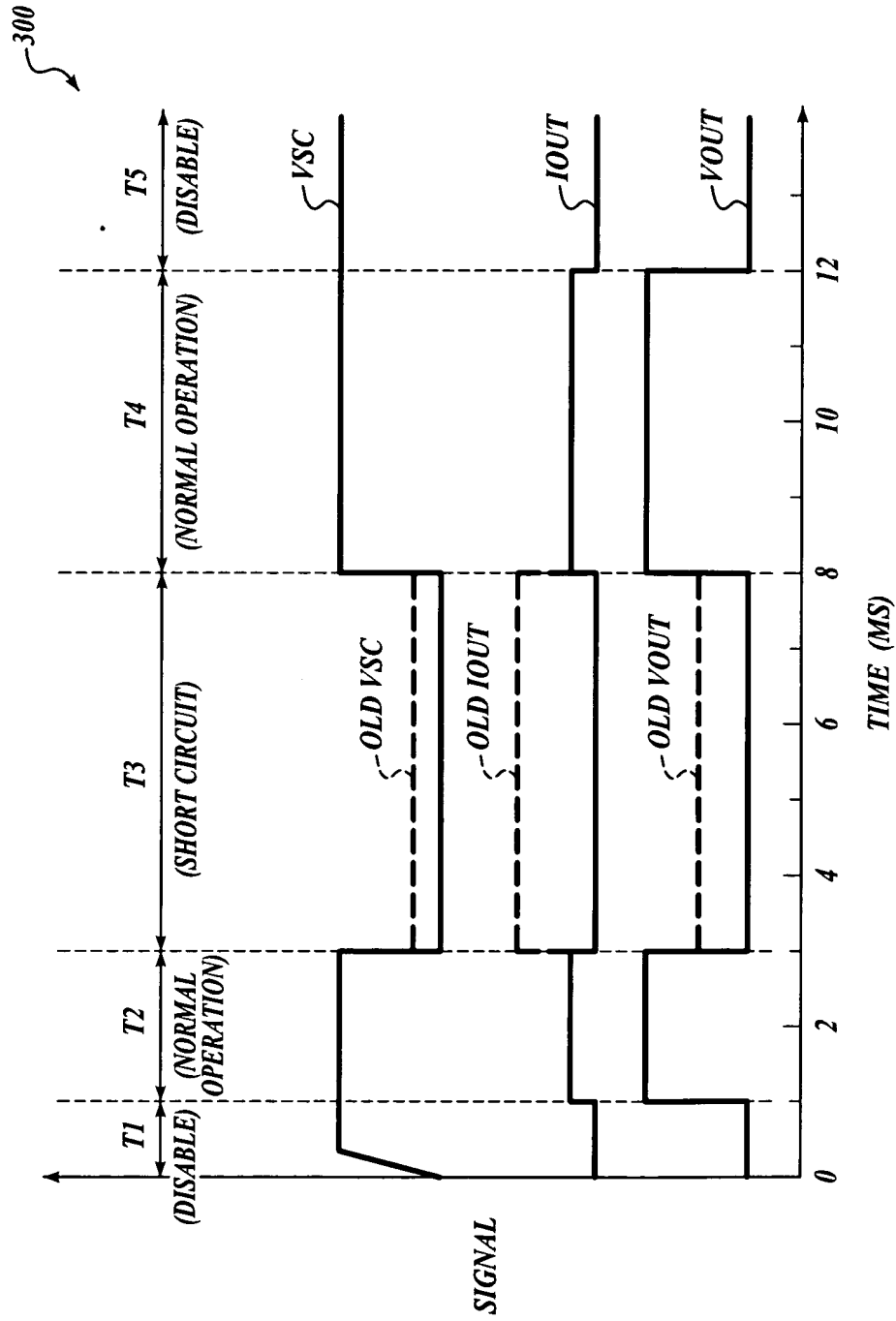


FIGURE 3